IN THE CLAIMS

Please amend the claims as follows:

1. (Original): A method for transmitting a control signal to an option pad of an integrated circuit chip at its package level comprising the steps of:

electrically isolating one of a plurality of commonly connected power transmitting pins of the integrated circuit package;

connecting the electrically isolated power transmitting pin to the option pad to thereby transmit a control signal from outside through the electrically isolated power transmitting pin to the option pad.

2. (Original): The method, as defined in claim 1, wherein the commonly connected power transmitting pins is connected to ground.

3. (Original): The method, as defined in claim 1, wherein the commonly connected power transmitting pins is connected to a power supply.

4. (Original): The method, as defined in claim 1, wherein the option pad is a pad for performing a burn-in test at the package level.

5. (Original): The method, as defined in claim 1, wherein the control signal is an external signal to perform a burn-in test at the package level.

6. (Original): The method, as defined in claim 1, wherein the control signal is an external signal to perform one of burn-in test, input/output test, and parallel bit test.

7. (Original): The method, as defined in claim 1, wherein the integrated circuit package includes a ball grid array pin arrangement.

8. (Original): The method, as defined in claim 1, wherein the integrated circuit chip includes a static random access memory device.

9. (Currently Amended): An integrated circuit package having an integrated circuit chip ~~for transmitting a test control signal from outside~~, comprising:

the integrated circuit chip being mounted in the integrated circuit package ~~with~~ comprising an option pad and a plurality of power pads connected with ~~an option pad and~~ power lines connected to an internal circuit;

power transmitting group pins connected to the power pads of a plurality of power transmitting pins assigned and formed at the integrated circuit package; and

at least one signal transmitting pin connected to the option pad but electrically isolated from the power transmitting group pins for transmitting a test control signal to the option pad.

10. (Original): The structure, as defined in claim 9, wherein the power pads are ground voltage pads when the power transmitting pins are ground voltage pins.

11. (Original): The structure, as defined in claim 9, wherein the power pads are power supply voltage pads when the power transmitting group pins are supply power voltage pins.

12. (Original): The structure, as defined in claim 9, wherein the option pad is a pad for performing a burn-in test at the package level.

13. (Original): The structure, as defined in claim 9, wherein the control signal is an external signal to perform a burn-in test at the package level.

14. (Original): The structure, as defined in claim 9, wherein the control signal is an external signal to perform one of burn-in test, input/output test, and parallel bit test.

15. (Original): The structure, as defined in claim 9, wherein the integrated circuit package includes a ball grid array pin arrangement.

16. (Original): The structure, as defined in claim 9, wherein the integrated circuit chip includes a static random access memory device.

17. (Original): The structure, as defined in claim 9, wherein the option pad includes an electric static discharge circuit.

18. (Original): The structure, as defined in claim 9, wherein the option pad includes a keeper circuit to prevent a false operation of a device when the signal transmitting pin is open.

19. (Original): The structure, as defined in claim 9, wherein the internal circuit is constructed with an option receiver having an inverter structure.

20. (Original): A method for performing a test by controlling an internal circuit of a package chip at the package level, comprising the steps of:

connecting a power transmitting pin to an option pad, the option pad being accessible only at the wafer level;

isolating the power transmitting pin from a plurality of power transmitting pins commonly connected to one of power and ground; and

transmitting a test control signal to the option pad through the power transmitting pin.

21. (New): The method, as defined in claim 1, further comprising the step of preventing a false operation of a device when the electrically isolated power transmitting pin is open.

22. (New): The method, as defined in claim 20, further comprising the step of preventing a false operation of a device when the electrically isolated power transmitting pin is open.